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## **OPTICAL PRINTING HEAD**

**15 [Abstract]**

**PURPOSE:** To enhance high speed recording properties and reliability by a method wherein a plurality of the light emitting data signals transmitted from a shift register are held for a definite period in one element of a drive circuit constituted of a membrane transistor and electric field light emitting elements are allowed to emit light two or more times.

**CONSTITUTION:** In an optical printing head constituted by a large number of electric field light emitting elements EL1-EL4... are arranged in a line form, one light emitting element, for example, EL1 is driven by a shift register SR, latches L1, L2, AND circuits A1-A3 to the held data in the latches, an OR circuit 01, an exclusive OR circuit EX1 and a voltage applying gate G1 to

**constitute one element. A low rank bit is held to the latch of an odd number among two latches in each element and the gradation display data of an upper rank bit is held to the latch of an even number and the electric field light emitting elements are allowed to emit light two or more times in the**

**5 light emitting number of times corresponding to a plurality of held light emitting data.**

**[Claims]**

1. An optical printing head having a driving circuit composed of an electro-luminescent device and a thin film transistor for driving the electro-luminescent device, in which a first element of the driving circuit constructed by the thin film transistor maintains a shift register and a plurality of luminescent data signals transmitted from the shift register for a certain time, and the optical printing head comprises one electro-luminescent device, a plurality of luminescent data memory devices, a plurality of luminescent pulse timing control lines, a plurality of logic devices for performing a logic operation between a plurality of luminescent pulse timing control signals outputted from the plurality of luminescent pulse timing control lines and a plurality of luminescent data signals maintained in the plurality of luminescent data memory devices for a certain period, a logic device for performing a logic operation between the data and a frame signal, and a luminescent voltage applying gate for applying a voltage to a data electrode of the electro-luminescent device based on a logic value of the logic device, and the electro-luminescent device emits light several times by the number of times of emission according to the plurality of luminescent data maintained in the luminescent data memory device for a certain period.

**[Title of the Invention]**

**OPTICAL PRINTING HEAD**

**[Detailed Description of the Invention]**

The present invention relates to a printing head using a light emitting

5 device, and more particularly, to a method for constructing a driving circuit  
of an optical printing head using an electro-luminescent device (hereinafter,  
an EL light emitting device).

**[Field of the Invention]**

10 **[Description of the Prior Art]**

An information processing device such as a copier, a facsimile, a computer, etc. is being drastically presented on the market, and the device requires a cheap cost, a high quality, and a high function. Especially, an information processing device for a personal use requires the above 15 characteristics much more. An optical printing head is a device used to irradiate light onto a photosensitive body inside the copier, the facsimile, the computer, etc. An EL light emitting device that can be easily minimized is being spotlighted as a light emitting device of the optical printing head.

The conventional optical printing head using the EL light emitting 20 device is shown in FIGURE 6. As shown in FIGURE 6, a plurality of EL light emitting devices are displayed as a capacity signal and each device has two electrodes. Each one electrode (a data electrode) of the plurality of EL light emitting devices (EL1 to EL16) arranged in a straight line is connected to an EL data driver 62 as a unit of adjacent plural electrodes. One electrode is 25 connected to a common electrode extended in a longitudinal direction of a

main scan direction of an EL printing head, and the electrode is connected to an EL common driver 63.

FIGURE 7 shows an example of a timing chart for inputting a driving pulse for driving the EL printing head shown in FIGURE 6. The light emitting device emits light four times during a recording period for one line. From the EL common driver, a plus pulse and a minus pulse are sequentially inputted to common driving lines Ca, Cb, Cc, and Cd. Also, pulses are inputted to data driving lines from the EL data driver. An emission and a non-emission of each EL light emitting device are determined by an overlap of the two voltages. As shown in FIGURE 7, if EL1 to EL4 do not emit light during the recording period for one line, a pulse having the same phase as the common side is inputted to Da. On the contrary, if EL5 to EL8 emit light, a pulse having an inverse phase to the common side is inputted to Db. Referring to EL9 to EL16, EL9, EL11, and EL14 emit light and Dc and Dd are used. A positive pulse and a negative pulse corresponding to approximately 200V are applied to the common side, and a pulse corresponding to approximately 20V is applied to the data side. Generally, a matrix driving method is used to drive the EL printing head.

However, a thin film transistor TFT that can be easily formed is being mainly used as the driving circuit. A data side driving circuit using the TFT enables a direct driving method more simple than a data inputting method, and enables data to be inputted with a high speed. Also, a printer using the EL light emitting device and the TFT driving circuit is easily maintained, has a compact characteristic, and requires no polygonal mirror in a laser print.

However, in case of a gray-scale recording using the direct driving

method, the number of times that an EL light emitting device emits light is controlled so that the EL light emitting device having a gray-scale can upgrade data several times during the recording period for one line. For example, in order to control the number of times that the EL light emitting

5 device emits light as four times (except non-emission) by the conventional circuit, data has to be inputted four times by replacement during the recording period for one line. When the number of times that data is inputted during the recording period for one line is less, the data is concentrated onto a specific part during the recording period for one line and an emission

10 of the EL light emitting device is non-uniformly generated.

As the result, a stress for the EL light emitting device is increased thereby to lower the lifespan of the EL light emitting device and to cause a minute change in the emission of the EL light emitting device.

By upgrading data frequently during the recording period for one line,

15 the non-uniform emission can be prevented. However, since a driving frequency of a shift register formed by the TFT is low as approximately 10MHz, the number of terminals for inputting data for the light emitting device has to be increased. As the result, a fast recording is not performed, a data processing prior to an input operation is complicated, and the

20 printing head has a complicated construction.

The present invention is to provide a gray scale-recordable optical printing head capable of reducing the number of times that data is transmitted during a recording period for one line and capable of providing a light emitting pattern that does not increase a stress for an EL light emitting

25 device.

**[Means for Solving the Problem]**

An optical printing head according to the present invention has a driving circuit composed of an electro-luminescent device and a thin film

5 transistor for driving the electro-luminescent device, in which a first element of the driving circuit constructed by the thin film transistor maintains a shift register and a plurality of luminescent data signals transmitted from the shift register for a certain time. The optical printing head comprises one electro-luminescent device, a plurality of luminescent data memory devices, a

10 plurality of luminescent pulse timing control lines, a plurality of logic devices for performing a logic operation between a plurality of luminescent pulse timing control signals outputted from the plurality of luminescent pulse timing control lines and a plurality of luminescent data signals maintained in the plurality of luminescent data memory devices for a certain

15 period, a logic device for performing a logic operation between the data and a frame signal, and a luminescent voltage applying gate for applying a voltage to a data electrode of the electro-luminescent device based on a logic value of the logic device, and the electro-luminescent device emits light several times by the number of times of emission according to the

20 plurality of luminescent data maintained in the luminescent data memory device for a certain period.

The shift register relevant to the optical printing head of the present invention sequentially transmits luminescent pulse data of each light emitting device inputted from an external circuit to adjacent driving elements.

The luminescent data memory device is a latch, receives a latch signal from an external circuit, applies the latch to the luminescent pulse data inputted from the shift register thereby to maintain the luminescent pulse data, and transmits the data to the logic device. In the present 5 invention, each EL light emitting device maintains gray-scale data, so that one EL light emitting device requires at least two latches.

The luminescent pulse timing control line is a control signal line applied from outside, and is controlled so that a luminescent pulse corresponding to each gray-scale can be spread during the recording period 10 for one line.

The logic device is composed of an AND circuit, an OR circuit, and an exclusive logic circuit. The logic device performs an operation between data maintained by the latch and the control signal applied from outside by the AND circuit and the OR circuit, and then performs an operation between 15 the data and a frame signal by the exclusive logic circuit. Also, the logic device transmits a constant voltage H pulse signal or a negative voltage L pulse signal to a voltage controlling gate.

The luminescent voltage applying gate receives the H pulse or the L pulse resulting from the operation. In case of receiving the H pulse, the 20 luminescent voltage applying gate applies an inverse pulse to a common side pulse to the EL light emitting device, and in case of receiving the L pulse, the luminescent voltage applying gate applies the same pulse as the common side pulse to the EL light emitting device.

The EL light emitting device receives a common side pulse voltage 25 applied to a common electrode and a data side pulse voltage applied to a

data side electrode as an inverse phase or the same phase to/as the common side pulse voltage, thereby performing an emission operation or a non-emission operation. By the operation, the EL light emitting device emits light several times by the number of times of an emission according to the

5 plurality of luminescent data maintained in the luminescent data memory device for a certain period.

The present invention can be also applied to a facsimile, a recording unit of a digital copier, etc.

10 [Means for Solving the Problem]

In the present invention, each EL light emitting device maintains a corresponding gray-scale data. Therefore, emission data or non-emission data needs not to be transmitted whenever a luminescent pulse is inputted or several pulses corresponding to a gray-scale are inputted. Since data can  
15 be consecutively inputted to adjacent EL light emitting devices, data prior to an input operation is easily processed. Also, in the present invention, the optical printer head has an excellent recording characteristic that a luminescent pulse is not concentrated onto a specific part during the recording period for one line.

20 [Preferred embodiment]

A preferred embodiment of the present invention will be explained with reference to FIGURES 1 to 5.

FIGURE 1 is a block diagram showing an optical printing head according to the present invention. Even if four light emitting devices were  
25 disclosed in FIGURE 1, thousands of EL light emitting devices are provided

at the optical printing head. A plurality of EL light emitting devices are arranged in a line unit (EL1 to EL4), one light emitting device, for example, EL1 is driven by a shift register SR, a plurality of latches, L1 and L2, AND circuits such as A1, A2, and A3 for maintaining data at the latches, an OR circuit O1, an exclusive logic circuit EX1, and a voltage applying gate G1, thereby constituting a first element. Luminescent data of each luminescent device transmits the shift register, SR and then is maintained by the latches L1 to L8.

5      circuit O1, an exclusive logic circuit EX1, and a voltage applying gate G1, thereby constituting a first element. Luminescent data of each luminescent device transmits the shift register, SR and then is maintained by the latches L1 to L8.

Gray-scale display data of a low bit is maintained at the odd numbered of latch among two latches of one light emitting device, and gray-scale display data of an upper bit is maintained at the even numbered of latch among two latches of one light emitting device. A non-emission is also applied to the above case, thereby displaying four gray scales. While the EL1 to EL4 are driven during the recording period for one line by the latches L1 to L8, a gray-scale display data, a low bit, an upper bit, and a shift register can be transmitted to the next one line.

10     numbered of latch among two latches of one light emitting device, and gray-scale display data of an upper bit is maintained at the even numbered of latch among two latches of one light emitting device. A non-emission is also applied to the above case, thereby displaying four gray scales. While the EL1 to EL4 are driven during the recording period for one line by the latches L1 to L8, a gray-scale display data, a low bit, an upper bit, and a shift register can be transmitted to the next one line.

15     L1 to L8, a gray-scale display data, a low bit, an upper bit, and a shift register can be transmitted to the next one line.

The number of the shift registers become two times for the gray-scale data, but does not re-transmit data corresponding to a gray-scale display for the recording period for one line thereby to correspond to a fast printing. Data maintained by the latches L1 to L8 is operated by control signals CTL1 and CTL2 applied from outside, and then is summed with a frame signal FR by an exclusive logical circuit, thereby opening and closing G4 by the voltage controlling gate G1. Due to the exclusive logic circuit EX1, a voltage having the same phase or an inverse phase as/to the frame signal FR can be applied to the EL light emitting device by the gray-scale data

20     printing. Data maintained by the latches L1 to L8 is operated by control signals CTL1 and CTL2 applied from outside, and then is summed with a frame signal FR by an exclusive logical circuit, thereby opening and closing G4 by the voltage controlling gate G1. Due to the exclusive logic circuit EX1, a voltage having the same phase or an inverse phase as/to the frame signal FR can be applied to the EL light emitting device by the gray-scale data

25     FR can be applied to the EL light emitting device by the gray-scale data

maintained at the latch. A voltage  $V_c$  is applied to common side electrodes of the EL1 to EL4 of the EL light emitting device, and a voltage having an inverse phase to the voltage  $V_c$  is applied to a data side electrode of the EL light emitting device. When the voltages applied to both ends of the EL light  
5 emitting device exceed threshold values, the EL light emitting device emits light.

FIGURE 2 is a timing chart of a signal when a circuit is operated, in which a luminescent period for one line is shown. As six positive pulses and six negative pulses are applied to the common side electrode of the EL light  
10 emitting device, a voltage having an inverse phase to the common side electrode is applied to the data side electrode. By the sum between the voltages applied to the data side electrode and the common side electrode, the EL light emitting device emits light. When a voltage more than a threshold is applied to the data side electrode, the EL light emitting device  
15 emits light 12 times to the maximum. If one data having two values exists at two latches corresponding to one light emitting device, the AND circuit of A2, A5, A8, and A11 is outputted as a high level and thereby a signal having an inverse phase to the FR signal is introduced into the G1 or G4. As the result, an inverse signal is outputted from the gate and thereby a voltage having  
20 the same phase as the FR signal is applied to the data side electrode of the EL light emitting device. Since the FR signal is introduced into the G1 to G4 as an inverse phase to the common side electrode, the EL light emitting device emits light. Maintenance data of the two latches is expressed as a low bit and an upper bit, and FIGURE 2 shows how a voltage is applied to the  
25 data side electrode of the EL emitting device by signals of CTL1 and CTL2.

As shown in FIGURE 2, when the EL light emitting device emits light 12 times for the latch data (1, 1), the device emits light 8 times for the latch data (0, 1) and emits light 4 times for the latch data (1, 0). That is, when numbers 1 to 12 are given to the common side pulse, the device emits light 12 times in

5 1 to 12 in case of the latch data (1, 1), 8 times in 1, 4, 5, 6, 7, 8, 9, and 12 in case of the latch data (0, 1), and 4 times in 1, 4, 7, and 10 in case of the latch data (1, 0).

The control signals CTL1 and CTL2 are selected so that a luminescent pulse corresponding to each gray-scale can be spread between

10 the recording period for one line. As the luminescent pulse, a pattern to be spread within a range of the recording period for one line is preferably used. However, the luminescent pulse is not limited to the pattern.

In the conventional circuit, data transmission of 9 times is necessary as shown in FIGURE 2 as the arrows because data maintained by the latch

15 has to be changed when levels of (1, 1), (0, 1), and (1, 0) are transited into a state different from an inverse state to the previous state at the time of reversing an FR signal. In the circuit of the present invention, data may be transmitted only first single time, and the time required to transmit data is greatly reduced when the number of shift registers is increased into two

20 times. As the number of gray-scales is increased, the effect that the plurality of latches are applied is increased.

In case of using a TFT as the driving circuit, the shift register, the latch, the AND circuit, the OR circuit, the exclusive logic circuit, etc. can be formed as a comparatively small device. On the contrary, a voltage applying

25 gate to the EL electrode of a final end has to satisfy a pressure resistant

characteristic and a current resistant characteristic thereby to be formed as a comparatively large size. Accordingly, the device having the plural latches and an occupied area thereof may be comparatively small.

Another embodiment of the present invention is illustrated in FIGURES 3 and 4. Referring to FIGURES 3 and 4, the number of the shift register is not increased when compared with the conventional circuit. However, the shift register has a latch, Lcn besides two latches for displaying a gray-scale, Lan and Lbn (n= 1 to 3). Data for upper bits of gray-scale data of each light emitting device is transmitted to the shift register thereby to be maintained in the LC1 to LC3. Then, data for lower bits is transmitted to the shift register. As a Latch-B signal and a Latch-A signal are sequentially applied to the shift register, the data maintained in the Lc1, etc. is transmitted to the La1 to La3. Then, as a Latch-C signal and a Latch-B signal are sequentially applied to the shift register, the data for lower bits of the gray-scale data is maintained in the Lb1 to Lb3.

FIGURE 4 is a timing chart. Referring to FIGURE 4, tn-1, tn, and tn+1 respectively denote a printing time of an n-1<sup>th</sup> line, an n<sup>th</sup> line, and an n+1<sup>th</sup> line. For the printing time of the tn-1 line, printing data of the next line is supplied. Upper bits and lower bits of the gray-scale are sequentially transmitted to the shift register by using 1/2 of the recording period for one line. The upper bit data and the lower bit data are maintained in the La1 to La3 and Lb1 to Lb3 at an initial time of the next printing period, and the luminescent pulse is controlled by the control lines, CTL1 and CTL2 for the data. In this embodiment, the light emitting device has 14 luminescent pulses for one line, and the first 12 pulses are controlled by printing data of

the line and the last 2 pulses are controlled by upper bits among the printing data of the next line.

The next upper bits tend to be 1 in consecutive lines, etc., and the line can be clarified by inputting two pulses. On the contrary, at the time of separating the line per each dot, two pulses are not inputted. Since upper bits of the next line are maintained in the Lc1 to Lc3 at a later time of the printing time for one line, the pulses can be controlled by the data by using the control line, CTL3. In case that the pulses are not controlled in the next line, the CTL3 is certified and the AND circuit for the output of the Lc1 to Lc3 is certified thereby to perform the aforementioned control (in this case, the Lc1 to Lc3 are necessary as buffers of read data). FIGURE 5 is an example showing a brightness voltage characteristic of the EL light emitting device. Referring to FIGURE 5, Vth denotes a luminescent threshold voltage. Also, at the time of driving the device, and a positive pulse and a negative pulse of a voltage of Va are applied to the EL light emitting device by the data side electrode and the common side electrode. However, since a pulse having a voltage less than the Vth is applied to a non-luminescent EL device, the non-luminescent EL device does not emit light.

20 [Effect of the Invention]

The optical printing head according to the present invention comprises a driving circuit composed of an electro-luminescent device and a thin film transistor for driving the electro-luminescent device, in which a first element of the driving circuit constructed by the thin film transistor maintains a shift register and a plurality of luminescent data signals

transmitted from the shift register for a certain time, and the optical printing head comprises one electro-luminescent device, a plurality of luminescent data memory devices, a plurality of luminescent pulse timing control lines, a plurality of logic devices for performing a logic operation between a plurality  
5 of luminescent pulse timing control signals outputted from the plurality of luminescent pulse timing control lines and a plurality of luminescent data signals maintained in the plurality of luminescent data memory devices for a certain period, a logic device for performing a logic operation between the data and a frame signal, and a luminescent voltage applying gate for  
10 applying a voltage to a data electrode of the electro-luminescent device based on a logic value of the logic device. In the optical printing head, the electro-luminescent device emits light several times by the number of times of an emission according to the plurality of luminescent data maintained in the luminescent data memory device for a certain period. Accordingly, a  
15 plurality of luminescent pulses can be set by spread for the recording period for one line without increasing the number of times that data is transmitted at the time of expressing a gray-scale. As the result, the optical printing head using the EL light emitting device having a fast recording characteristic, a reliability, and a high recording quality can be implemented.  
20 The optical printing head is very suitable for a fast printing for an output of an information processing device such as a copier, a facsimile, a computer, etc. that is being minimized with a high function.

[Description of Drawings]

25 FIGURE 1 is a block diagram showing a first embodiment of an

**optical printing head according to the present invention;**

**FIGURE 2 is a view showing a driving timing chart of the optical printing head according to the first embodiment of the present invention;**

**FIGURE 3 is a block diagram showing another embodiment of the**  
**5 optical printing head according to the present invention;**

**FIGURE 4 is a view showing a driving timing chart of the optical printing head according to another embodiment of the present invention;**

**FIGURE 5 is a view showing an example of a brightness voltage characteristic of the optical printing head according to the present**  
**10 invention;**

**FIGURE 6 is a block diagram showing a main part of an optical printing head in accordance with the conventional art; and**

**FIGURE 7 is a view showing a driving timing chart of the optical printing head in accordance with the conventional art.**